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I Claim:

1. A method of making a dielectrically isolated integrated circuit comprising the steps of:

providing a substrate having a principal surface;

forming an etch barrier layer in the substrate parallel to the principal surface;

forming semiconductor devices on the principal surface;

after forming the semiconductor devices, depositing a low stress insulating membrane over the semiconductor devices; and

etching away to the etch barrier layer a portion of the substrate from a backside of the substrate opposite the principal surface.

2. The method of Claim 1, further comprising the steps of:

forming an epitaxial layer on the principal surface; and

forming the semiconductor devices in the epitaxial layer.

3. The method of Claim 1, further comprising the step of forming a trench in the substrate isolating at least one of the semiconductor devices from the others.

4. The method of Claim 1, wherein the etch barrier layer is formed lying less than 50 μm below the principal surface.

5. The method of Claim 1, further comprising the step of forming conductors in the insulating membrane for interconnecting the semiconductor devices.

6. The method of Claim 1, wherein the step of etching away comprises the step of leaving an edge portion of the substrate unetched, thereby supporting a central etched away portion of the substrate.

7. The method of Claim 1, further comprising the step of attaching an annular support ring to an edge portion of the substrate.

8. The method of Claim 1, wherein the step of depositing includes the step of supplying $SiH_4$ gas, $N_2O$ gas, and $N_2$ gas at a temperature of about 400°C.

9. The method of Claim 1, wherein the step of depositing includes the step of supplying $SiH_4$ gas, $NH_3$ gas, and $N_2$ gas at a temperature of about 400°C.

10. The method of Claim 1, wherein the step of forming an etch barrier layer comprises:

implanting a lightly doped etch stop barrier layer, wherein the implanted material is one of oxygen or nitrogen.

11. The method of Claim 1, wherein the step of providing comprises the steps of:

providing a semiconductor substrate;

doping an etch stop layer in the substrate;

epitaxially growing a germanium-semiconductor material layer on a surface of the substrate; and

etching the substrate to remove the germanium-semiconductor material layer and the etch stop layer, thereby forming the semiconductor layer.

12. A method of making an integrated circuit comprising the steps of:

forming a substrate having a thickness of less than about 50 μm;

forming semiconductor devices on a principal surface of the substrate;

depositing a low stress insulating membrane over the semiconductor devices; and

forming electrical interconnections in the membrane extending between the semiconductor devices.

13. The method of Claim 12, further comprising the steps of:

forming an epitaxial layer on the principal surface; and

forming the semiconductor devices in the epitaxial layer.

14. The method of Claim 12, further comprising the step of forming a trench in the substrate isolating at least one of the semiconductor devices from the others.

15. The method of Claim 12, wherein the step of the forming the substrate comprises electro-chemical etching.

16. The method of Claim 12, wherein the step of depositing includes the step of supplying $SiH_4$ gas, $N_2$ gas, and $N_2O$ gas at a temperature of about 400°C.

17. The method of Claim 12, wherein the step of depositing includes the step of supplying $SiH_4$ gas, $NH_3$ gas and $N_2$ gas, at a temperature of about 400°C.

18. The method of Claim 1, further comprising the steps of:

forming an additional thickness of low stress insulating material over the membrane; and

forming a plurality of recesses in the additional thickness.

19. A method for forming a flat panel display comprising the steps of:

providing a substrate;

forming a layer of a release agent on a surface of the substrate;

forming a membrane less than about 100 μm thick and including integrated circuitry on the layer of release agent;

selectively depositing color phosphors on localized portions of the membrane, thereby forming pixels; and

releasing the membrane from the substrate by activating the release agent.

20. The method of Claim 19, wherein the step of selectively depositing comprises electro-phoretic plating of individual color phosphors.

21. The method of Claim 19, further comprising the step of attaching integrated circuit die to the membrane, the die being electrically connected to the integrated circuits in the membrane.

22. A method of making a stacked integrated circuit structure comprising the steps of:

forming first and second flexible membranes each including a plurality of electrically interconnected semiconductor devices;

bonding a principal surface of the first flexible membrane to the second flexible membrane; and

interconnecting at least one semiconductor

device in the first flexible membrane to a semiconductor device in the second flexible membrane.

23. The method of Claim 22, further including the step, prior to bonding, of aligning the first and second flexible membranes by observing optical alignment marks on one of the flexible membranes.

24. The method of Claim 22 wherein at least some of the semiconductor devices are optical devices, and the step of interconnecting includes the steps of:

forming vias in each flexible membrane, the vias each being associated with one of the optical devices; and

aligning the vias in the first flexible membrane with the vias in the second flexible membrane, thereby forming waveguides for connecting the optical devices.

25. A method of testing an integrated circuit having electrical contracts formed thereon spaced apart a distance of less than about 50 μm, comprising the steps of:

providing a flexible tester membrane including a plurality of probe points formed on one surface thereof, and a plurality of integrated circuits attached to an opposing surface thereof for providing test signals to the probe points;

electrically interconnecting the integrated circuits to the probe points by conductors extending through the tester membrane: and

providing at least two of the probe points spaced apart less than about 50 μm.

26. The device of Claim 25, wherein at least two of

the probe points are spaced apart by less than about 2 μm.

27. An integrated circuit assembly comprising:

a plurality of vertically stacked flexible membranes each having semiconductor devices and interconnections between the semiconductor devices formed on the membrane;

an array of optical transmitter semiconductor devices formed on one of the membranes; and

an array of optical receiver semiconductor devices formed on a second of the membranes and aligned with the array of optical transmitter devices to receive optical transmissions of data therefrom.

28. The device of Claim 27, further comprising a second array of optical receiver semiconductor devices formed on one of the membranes for receiving optical transmissions from an external transmitter.

29. The device of Claim 27, wherein at least one of the membranes includes a transparent receiver for receiving the optical transmissions and simultaneously passively propagating the optical transmissions through the at least one membrane.

30. A method of making an integrated circuit interconnect membrane comprising:

providing a substrate having a planner principal surface;

coating the principal surface with a release agent;

forming a flexible dielectric membrane on the release agent;

forming conducting traces on the membrane;

attaching integrated circuits to the conducting

traces; and

releasing the membrane from the substrate by activating the release agent.

31. A lift-off method of forming a conductive metal trace in a flexible membrane for electrical interconnection of integrated circuits mounted on the membrane, comprising the steps of:

forming a resist layer on a surface of the membrane;

patterning the resist layer, exposing a portion of the surface;

isotopically etching the portion of the membrane at the exposed surface portion thereof, undercutting the resist layer and forming a groove in the membrane;

depositing a layer of metal over the resist layer and in the groove;

removing the resist layer and overlying metal layer; and

forming a dielectric layer overlying the groove.

32. A method of forming a field effect transistor having a narrow gate and opposed gate contact, comprising the steps of:

forming a silicon layer less than about 10 μm thick;

forming a gate electrode over the principal surface of the silicon layer;

forming a low stress dielectric layer less than about 10 μm thick over the silicon layer and over the gate electrode;

forming doped regions in the silicon layer;

etching a groove in the silicon layer from the surface opposing the principal surface thereof in a

portion of the silicon layer underlying the gate electrode;

depositing metal in the groove to a predetermined depth;

etching away the opposing surface of the silicon layer to the predetermined depth;

depositing a mask layer on the etched-away surface;

patterning the mask layer, thereby exposing portions of the etched-away surface;

forming additional doped regions in the silicon layer at the exposed portions of the etched-away surface;

removing the mask layer; and

etching away additional portions the etched-away surface to the bottom of the groove, thereby removing all of the deposited metal.

33. The method of Claim 32, further comprising the steps of forming a trench in the silicon layer surrounding the active portion of the transistor.

34. A method of forming a multi-chip module using a flexible membrane to interconnect the chips, comprising the steps of:

providing a flexible membrane;

forming conductive traces on the membrane; and

mounting a plurality of integrated circuit die to the membrane at the traces.

35. The method of Claim 34, further comprising the steps of:

forming a dielectric layer on the membrane; and

forming additional metal traces on the dielectric layer.

36. The method of Claim 34, further comprising the step of providing a support ring attached to the edge of the membrane.

37. The method of Claim 36, wherein the step of mounting comprises the steps of:

enclosing the membrane and support ring in a housing; and

providing pressure in the housing to keep the membrane in contact with the integrated circuit die.

38. The method of Claim 34, further comprising the step of forming a hermetic seal between a surface of each die and the membrane.

39. The method of Claim 34, wherein the step of mounting comprises the steps of:

providing a plurality of recesses in a surface of the membrane, each recess being associated with a bonding pad on one of the integrated circuit die;

providing a solder bump on one of each bonding pad or the bottom of the associated recess; and

forming a solder weld bond between each bonding pad and the associated recess by applying heat to the membrane.

40. The method of Claim 39, wherein the heat is applied to a surface of the membrane opposite to that in which the recesses are formed.

41. The method of Claim 39, wherein the die bonding pads are each less than about 2 mils in diameter.

42. A method of bonding an integrated circuit die to a flexible membrane, comprising the steps of:

providing an integrated circuit die having at least one bonding pad formed overlying semiconductor devices of the integrated circuit die; and

attaching the integrated circuit die to the flexible membrane by bonding the bonding pads to electrical traces on the membrane.

43. The method of Claim 42, wherein the step of attaching comprises:

pressing the integrated circuit die against a surface of the membrane;

providing solder at a point to be bonded;

applying pressure to an opposing surface of the membrane; and

heating the opposing surface of the membrane.

44. The method of Claim 43, further comprising the step of hermetically bonding an edge of the integrated circuit die to the membrane.

45. A method of aligning a lithographic fabrication tool to a substrate to be exposed by the tool, comprising the steps of:

providing a first conductive coil pattern on a surface of the substrate;

applying electrical current to the coil pattern;

providing a second conductive coil on a surface of the tool;

bringing the surface of the tool near to the surface of the substrate; and

sensing an electromagnetic field generated by the first coil in the second coil.

46. The method of Claim 5, wherein the electrical current is provided from contacts on the tool that contact

the first coil.

47. A method of forming a transistor, comprising the steps of:

providing a flexible membrane having a thin film of semiconductor material formed on the membrane;

forming a trench in the semiconductor material;

doping portions of the semiconductor material;

laterally growing extensions of the sidewalls of the trench, thereby narrowing the trench to a predetermined width;

filling the remaining width of the trench with semiconductor material doped at a concentration differing from a doping level of the extensions; and

forming an electrical contact to the filled portion of the trench through the flexible membrane.

48. The method of Claim 47, further comprising the step of isolating the trench by forming additional trenches in the semiconductor material surrounding the first trench.

49. The method of Claim 47, further comprising the steps, prior to the step of laterally growing, of:

forming a mask layer over a principal surface of the thin film of semiconductor material;

etching away sidewalls of the trench, thereby forming a cavity under the mask layer; and

laterally growing a plurality of differently doped layers of semiconductor material on the sidewalls of the cavity.

50. A field effect transistor comprising:

a flexible dielectric membrane having a principal surface;

a semiconductor film formed on the principal surface of the membrane, the semiconductor film including at least three doped layers;

a contact to a first of the three doped layers formed through the membrane;

a contact to a second of the doped layers formed on a principal surface of the semiconductor film;

an insulating layer formed over an edge of the semiconductor film; and

a gate electrode formed overlying the insulating layer.

51. The device of Claim 50, wherein a portion of the third layer extends over edges of the first and second layers.

52. The device of Claim 1 wherein the third layer is located intermediate of the first and second layers, and a portion of the third layer extends over edges of the first and second layers, and

wherein the contact to the third layer overlies the extended portion of the third layer.

53. A bipolar transistor comprising:

a flexible dielectric membrane having a principal surface;

a semiconductor film formed on the principal surface and including at least three doped layers;

a contact to the first of the three layers formed through the membrane; and

contacts to the second and the third layers.

54. A method of forming an interconnect structure for a circuit membrane, comprising the steps of:

providing a semiconductor film;

forming a flexible dielectric membrane on a principal surface of the semiconductor film;

forming a layer of amorphous silicon on the membrane;

patterning the amorphous silicon layer to form trenches and vias therein;

depositing a layer of metal over the patterned amorphous silicon;

patterning the deposited layer of metal, thereby forming metal traces;

forming a second layer of amorphous silicon overlying the traces;

patterning the second layer of amorphous silicon;

forming a second dielectric layer over the second patterned layer of amorphous silicon;

forming etch vias penetrating the dielectric layer to the underlying second layer of amorphous silicon; and

removing the first and second layers of amorphous silicon through the etch vias, thereby leaving the metal traces supported at the vias by the dielectric membrane and overlain by the dielectric layer.

55. The method of Claim 4, further comprising the steps of:

forming additional metal traces supported on the dielectric layer; and

forming an additional dielectric layer overlying the additional metal traces.

56. The method of Claim 4, further comprising, after the step of forming the second layer of amorphous silicon, of depositing a layer of metal on the second layer of

amorphous silicon.

57. A method of fabricating an integrated circuit comprising the steps of:

providing a free standing membrane formed of a layer of low stress dielectric and a substrate layer;

forming a plurality of transistors in the substrate layer; and

forming interconnections on the dielectric layer between the transistors

58. A method of forming an interconnect circuit comprising the steps of:

providing a free standing membrane formed of at least one layer of low stress dielectric; and

forming a pattern of electrically conductive traces on the dielectric.

59. The method of Claim 58, wherein the step of providing comprises:

providing a dielectric substrate less than about 100 mils thick;

forming films of polycrystalline silicon on both surfaces of the substrate; and

etching away a portion of the substrate;

wherein the pattern of electrically conductive traces are formed by patterning a metal film deposited on at least one of the films of polycrystalline silicon.

60. A method of forming a field effect transistor comprising the steps of:

providing a membrane comprising a semiconductor layer overlying a low stress dielectric layer;

forming a drain region and a source region

laterally spaced apart from the drain region in the semiconductor layer, a portion of the semiconductor layer between the source and drain regions being a gate region;

forming an insulating layer overlying the semiconductor layer; and

forming a gate electrode on the insulating layer, one edge of the gate electrode being in a plane defined by an interface of one of the source region or the drain region and the gate region, and a second edge of the gate electrode extending over the other of the drain region or source region.

61. A method of forming a transistor comprising the steps of:

providing a flexible membrane including a low stress dielectric layer and a semiconductor layer;

forming a first and a second doped regions in the semiconductor layer, the first and second doped regions being vertically spaced apart and separated by a control region;

epitaxially growing an extension of the control region extending over an edge of the semiconductor layer and contacting edges of the first and second doped regions; and

forming electrical contacts to the first and second doped regions and to extension of the control region.

62. A method of testing an integrated circuit comprising:

providing a flexible free standing circuit membrane including a semiconductor layer and a flexible low stress dielectric layer, and having at least 100 probe points formed on its principal

surface;

providing a source of pressure against a back surface of the membrane, thereby contacting the integrated circuit being tested with the probe points; and

moving the integrated circuit being tested laterally relative to the circuit membrane while in contact with the probe points.

63. The method of Claim 62, wherein the lateral motion is less than about 100 μm and is repeated.

64. A semiconductor processing lithography apparatus for maskless pattern generation comprising:

an array of radiation source cells arranged in rows and columns, the array being formed on a flexible insulating membrane held in a support frame;

control logic mounted on the membrane for controlling the cells, wherein each cell comprises:

a source of radiation;

a target on which the radiation is incident for generating X-rays; and

an aperture for emitting the X-rays from the target onto a surface to be exposed.

65. The device of Claim 64, wherein each cell is in area less than about 50 μm by 50 μm.

66. The device of Claim 64, wherein the array includes at least one million cells.

67. A lithography pattern generating device comprising:

an array of cells arranged in rows and columns, the array being formed on a flexible insulating

membrane held in a support frame, each cell being individually controlled to permit passage of charged particles from an external source; and

control logic mounted on the membrane for controlling each cell;

wherein each cell comprises an aperture for emitting the particles onto a surface to be exposed.

68. A lithography pattern generating device comprising:

an array of cells arranged in rows and columns, the array being formed on a flexible insulating membrane held in a support frame, each cell defining an aperture to permit passage of charged particles from a source;

a movable shutter for covering each aperture; to block said passage; and

control logic mounted on the membrane for controlling movement of each shutter.

69. A contact stepper printer lithography method comprising:

providing a mask structure formed of a flexible membrane;

bringing the mask structure adjacent to a substrate to be patterned;

providing pressure against a backside of the mask structure thereby bringing a frontside of the mask structure to within a predetermined distance of the substrate;

exposing a first portion of the substrate to a source of radiation propagating through the mask structure;

moving the mask structure adjacent to a second portion of the substrate; and

exposing the second portion to the source of radiation propagating through the mask structure.

70. The method of Claim 69, wherein the predetermined distance is zero.

71. The method of Claim 69, further comprising the steps of:

providing electric coils on both the frontside of the mask structure and on the substrate; and

aligning the mask structure to the substrate by sensing an electric current present in a coil located on one of the mask structure and substrate in a coil located on the other of the mask structure and substrate.

72. The method of Claim 71, further comprising:

providing piezoelectric motion control for aligning the substrate relative to the mask structure in response to the sensed electric current.

73. A method of forming a lithographic fixed mask comprising the steps of:

providing a membrane including a semiconductor layer on a first low stress dielectric layer;

forming a metal layer on the semiconductor layer;

patterning the metal layer, thereby removing portions thereof;

selectively etching portions of the semiconductor layer underlying the removed portions of the metal layer;

depositing a second low stress dielectric layer over the patterned semiconductor layer; and

removing the first low stress dielectric layer.

74. A method of forming a fixed stencil lithographic mask comprising the steps of:

providing a membrane including a semiconductor layer on a low stress dielectric layer;

patterning the dielectric layer by etching away portions thereof; and

selectively wet etching the silicon layer to remove portions thereof.

75. A method of forming a sensor diaphragm comprising the steps of:

providing a semiconductor material substrate;

forming a low stress dielectric layer on the substrate; and

etching away a portion of the substrate, leaving a portion of the dielectric layer as a free standing diaphragm supported at its edges by the substrate.

76. The method of Claim 75, wherein the step of etching leaves a flexible layer of substrate material on the freestanding diaphragm.